Figure 1 depicts a block diagram of the sine wave generator where the first block in the process is the sample rate generator. The sample rate generator is responsible for generating a max sample rate count used to define the count rate needed to reach a desired frequency.

To determine the count rate needed to reach a desired frequency, we begin with the equation:

1/[Output Frequency of Sine Wave] = (Maximum Phase Counts) \* (Phase Increment Delay) (1)

The maximum phase counts is defined by the accumulator component which is 8-bits (8-bit phase resolution) and the phase increment delay is defined as multiplied by the max sample rate count. Eq (1) becomes

1/[Output Frequency of Sine Wave] =

and for a 100 MHz clock, we get

Solving for Max Sample Rate Count from Eq(2) gives

Max Sample Rate Count = 1/[Desired Output Frequency] \* 100 MHz \* 1/256

where 100 Mhz is the clock rate and 256 is the 8-bit accumulator size and Max Sample Rate Count determines how often the counter generates an enable pulse.

Example for 500Hz 🡪 Sample Rate Count(500Hz) = (1/500) \* 100MHz \* 1/256 = 781

Calculations of Max Sample Rate Count values and corresponding frequencies are found in Table 1.

Table 1: Max Sample Rate Count for Different Frequencies

|  |  |  |  |
| --- | --- | --- | --- |
| Desired Frequency |  | Max Sample Rate Count | Switch Selction(2:0) |
| 0 HZ |  | Special Case | 000 |
| 500Hz |  | (1/500) \* 100MHz \* 1/256 = 781 | 001 |
| 1000Hz |  | (1/1000) \* 100MHz \* 1/256 = 391 | 010 |
| 1500Hz |  | (1/1500) \* 100MHz \* 1/256 = 260 | 011 |
| 2000Hz |  | (1/2000) \* 100MHz \* 1/256 = 195 | 100 |
| 2500Hz |  | (1/2500) \* 100MHz \* 1/256 = 156 | 101 |
| 3000Hz |  | (1/3000) \* 100MHz \* 1/256 = 130 | 110 |
| 3500Hz |  | (1/3500) \* 100MHz \* 1/256 = 112 | 111 |

The eight different frequencies found in Table 1 are selectable by SW(2:0).

The VHDL implementation of the above values by the SW is done by a 8 to 1 Frequency Selection MUX to select an assigned Max Sample Rate Count value (MaxCnt)